

## ABSTRACT

A method and apparatus for high speed addressing of a memory space from a relatively small address space. An N-bit bus interfaces with a memory device having a  
5  $2^M$  address memory space, where M is greater than N. The method and apparatus provide for (a) providing at least two registers, (b) receiving one byte of a plurality of N-bit bytes that together define an address in the memory space, (c) incrementing a count as a result of completing step (b), (d) addressing one of the two registers according to the incremented count in step (c), and (e) storing the one byte in the register addressed in step  
10 (d).